APPARATUS AND METHOD FOR MANUFACTURING A SEMICONDUCTOR WAFER WITH REDUCED DELAMINATION AND PEELING

ABSTRACT OF THE DISCLOSURE

A multi-layered semiconductor structure with free areas limiting the placement of test keys. First and second scribe lines intersect to define one corner point of a die. The first and second scribe lines are part of the multilayered structure and at least one layer of the multi-layer structure is a low-k dielectric layer. Free area A_1 is defined on the first scribe line and is defined by the equation $A_1 = D_1 \times S_1$, where D_1 is the distance from the corner point of the die toward the main area of the die, and S_1 is the width of the first scribe line. Free area A_S is defined at the intersection of the first scribe line and the second scribe line adjacent the die and is defined by the equation $A_S = S_1 \times S_2$, where S_2 is the width of the second scribe line.